

PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER WITH TWO-POINT MODULATION

ABSTRACT OF THE DISCLOSURE

5 A phase-locked loop (PLL) frequency synthesizer having a two-point data modulation scheme and
ΣΔ modulator, fractional-N architecture. In the synthesizer, data are modulated at both the PLL frequency
divider and the voltage-controlled oscillator (VCO). The complementary frequency responses at these two
modulation points allow the PLL bandwidth to be sufficiently narrow to attenuate phase noise from the phase
detector, frequency divider, and ΣΔ quantization error, without adversely affecting the data. Fractional-N
10 architecture allows a large range of reference frequencies to be used with the PLL and high frequency
resolution of the output signal. The ΣΔ modulator modulates the feedback signal generated by the PLL
frequency divider with data and quantizes the spurious signals inherent in a fractional-N design to high
frequencies that the PLL loop filter can attenuate.

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